Approved 1/25/05 JHA

AMENDMENTS TO THE SPECIFICATION

Please substitute the following replacement paragraphs for the paragraphs that start at the specified page and line number of the present specification:

At page 10, line 8:

The comparand register 150 stores values that may be compared with data stored in the CAM array 110 in response to control signals from the instruction decoder 120. The comparand values stored in the comparand register 150 are also referred to as search keys. The comparand register 150 is coupled to the DBUS 141 and receives a search key from the DBUS 141. For alternative embodiments, the comparand register may be omitted. In response to a compare instruction, comparand register 150 provides the search key to CAM array 110 (e.g., over one or more comparand signal lines or, alternatively, over one or more of the data bit lines). CAM array 110 compares the search key against its entries and provides the match results on match lines 115 to priority encoder 160. Additionally, the match results may be provided to flag logic (not shown) that indicates whether there is a match, multiple match, full condition or the like. In response to the signals on the match lines,~~,~~ the priority encoder 160 generates an index or address of the row in the CAM array that stores information (masked or unmasked) that matches the search key and has the highest priority. Priority may be determined between entries in CAM array 110 by the physical location of the entries in the CAM array (i.e., by row number), or by explicit priorities assigned to each entry.

At page 11, line 1:

The compare logic 165 is coupled to the priority encoder 160 and the address counter 140. The compare logic 165 performs a comparison between an index output from the priority encoder 160 and a counter value output from the address counter 140, and generates the signal TFLAG whose logic state indicates the comparison result. Compare logic 165 may be particularly useful in performing BIST test sequences generated within the CAM Device 100 (e.g., by a control unit) or test sequences provided by external stimuli such as an ATE or other circuitry. Because ACTR 140 can be readily updated (e.g., either incremented or decremented) in response to one or more instructions decoded by instruction decoder 120, compare logic 165 can be used to flag test results for a number of tests that can be executed on CAM device 100 ~~is~~ in an efficient manner.

Some examples of the tests that can be executed on CAM device 100 utilizing compare logic 165 are illustrated below. However, many other tests may also be run on CAM device 100 utilizing compare logic 165, and scope of this application is not limited to only those examples described below.

At page 21, line 1:

Figure 7 is a block diagram of a CAM device 700 that includes the same components as in CAM devices 100 or 400, and further includes multiplexers 780 and 785. In response to a control signal from the instruction decoder 120, multiplexer 780 forwards either data from the DBUS 141 or a counter value from the address counter 140 to the comparand register 150. This allows the ~~compare circuit 155~~comparand register 150 to use a counter value from the address counter 140 as a search key. In response to a control signal from the instruction decoder 120, multiplexer 785 forwards either data from the DBUS 141 or a counter value from the address counter 140 to the write circuit 130. This allows the write circuit 130 to write a counter value from the address counter 140 into a row of CAM cells in the CAM array 110.